

Malla Reddy College of Engineering & Technology

(AUTONOMOUS INSTITUTION_UGC, GOVT.OF INDIA)

Affiliated to JNTUH; Approved by AICTE, NBA-Tier 1, NAAC with A-Grade, ISO 9001:2015



ONLINE FACULTY DEVELOPMENT PROGRAMME (FDP)

on

“NANOTECHNOLOGY FOR VLSI: FABRICATION AND CHALLENGES”

Organized by MRCET in association with E & ICT Academy NIT PATNA

Supported by

**Ministry of Electronics and Information Technology
(Meity), Govt. of India**

An online Faculty development programme on “**Nanotechnology for VLSI: Fabrication and Challenges**” was organised by **Malla Reddy college of Engineering & Technology** in association with **NIT Patna**, on FEB 3-7, 2025. During the FDP, Resource persons from Various IITs, NITs, IIITs and CSIR Laboratories were delivered insightful lectures and demonstrated their laboratory facilities with live examples of Nanomaterial’s synthesis and characterisation techniques. Complete schedule of FDP is provided in ANNEXURES

Heartfelt Thanks to our constant motivation **Shri Ch. Malla Reddy** sir, Chairman Malla Reddy Group of Institutions, **Dr. V.S.K. Reddy** Sir, Director, **Dr. S. Srinivasa Rao** sir, Principal, **Dr. Sesha Thalpa Sai** sir, Dean (R&D) and our vibrant HOD of H&S, **Dr V. Madhusudhana Reddy**, for giving an opportunity to organize the FDP

The FDP was started with an inaugural session on FEB 03, by co-ordinators **Dr. Pushpa Giri**, & **Dr. Jitendra Bahadur Maurya** at NIT Patna, and **Dr V. Madhusudhana Reddy** at MRCET, respectively, followed by other dignitaries.

About the Theme of the Programme

Nanotechnology plays a crucial role in VLSI fabrication by enabling the creation of incredibly small transistors and other electronic components on a single chip, achieved through the manipulation of matter at the atomic and molecular level, allowing for significantly increased circuit density and improved performance in microchips. To achieve these small features, advanced lithography techniques may be employed which use extremely short wavelengths of light to precisely pattern the circuit layout on the wafer. The nanotechnology offers a precise exposition of extremely thin layers of materials which is crucial for the nano scale structures on the wafer. Moreover, miniaturization reduces power consumption which will increase the durability of the device.

Session on

Recent Trends in Semiconductor Devices from Simulation, and Integration of Machine Learning Aspects

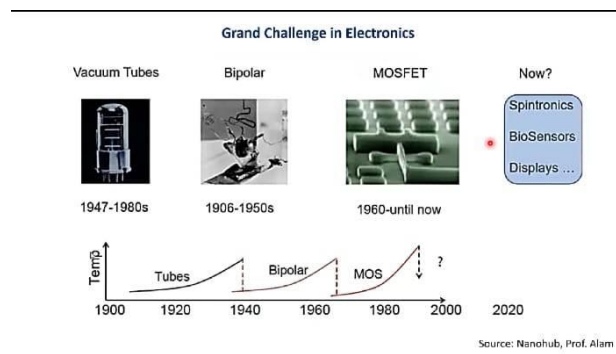
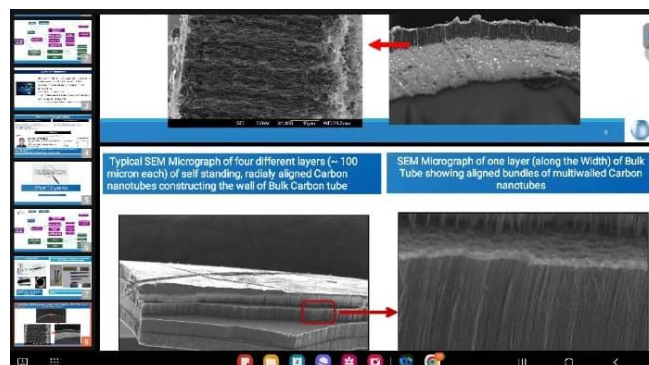
By:
Dr. Shashi Kant Sharma
Assistant Professor
Department of Electronics and Communication Engineering



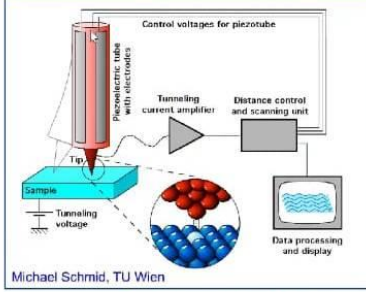
भारतीय सूचना प्रौद्योगिकी संस्थान राँची
INDIAN INSTITUTE OF INFORMATION TECHNOLOGY, RANCHI
(An Institute of National Importance under act of Parliament)
(Ranchi - 834010), Jharkhand, India



Dr. Shashi Kant Sharma • Unverified



Scanning Tunneling Microscopy (STM)



Control voltages for piezotube

Piezoelectric tube with electrodes

Tip

Sample

Tunneling voltage

Tunneling current amplifier

Distance control and scanning unit

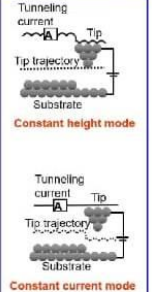
Data processing and display

Michael Schmid, TU Wien

$$I_t \propto V \exp(-A\phi^{1/2}d)$$

I_t : the tunnel current, a sensitive function of the gap width d ; V : the bias voltage; ϕ : the average barrier height (work function); A : constant = $1.025 \text{ eV}^{-1/2} \text{ \AA}^{-1}$.

Resolution limit: 0.1 nm (Lateral), 0.01 nm (Vertical)



Tunneling current

Tip trajectory

Substrate

Constant height mode

Tunneling current

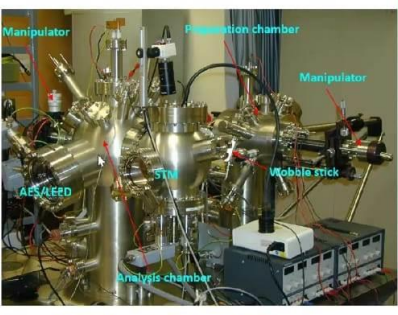
Tip trajectory

Substrate

Constant current mode

Operational Mode

Ultra-high vacuum STM system



Manipulator

Preparation chamber

Manipulator

Wobble stick

AES/LEED

STM

Analysis chamber

- Base Press
- Sb (mostly sources)
- Flux calibr electron spe
- Sample he
- STM image (RT)

Multi-chamber Omicron UHV system equipped with STM, LEED and AES

Every day, four sessions (two hours of each session) from morning 9 AM to 6 PM were presented by the guest speakers on various topics starting with *Advances in nanoscale CMOS technology, Chip-scale optoelectronic devices based on semiconductor heterojunctions, Emerging research trends in thin film technology based devices for electronics and photonics applications, etc., followed by live demonstrations of Synthesis and characterization of nanomaterials, Demonstration of sputtering, spin coating, and probe sputtering machines.*

Faculty and Researchers from MRCET, many universities, and Engineering colleges have registered for FDP and actively participated throughout the 5 days of FDP. Almost 100 participants were participated in FDP. The expertise and passion for the subject matter of the resource persons was truly impressive.

Feedback from participants was very positive & enriched with their understanding of nanotechnology and its applications in VLSI, and they are confident that the knowledge and insights gained will have a positive impact on teaching and research endeavours.

FDP BROUCHER

ONE-WEEK FDP INCLUDES

- 5-days training will be conducted by experts from India and abroad with experience ranging from several years to several decades in delivering sessions in India and abroad. The training hour is 5-6 hours each day. The mode of training is Instructor-led live online.
- 40 Hours of Instructor-led live online Hands-on learning & Interactive Query Sessions.
- Soft copy of study material, Training PPTs, recorded session & Project code
- E-certificates will be given to participants who have attended more than 70% of the workshop sessions and complete the assessment at the end of the FDP.
- **MODE OF CONDUCTION:** Online
- **TIMINGS:** Mon-Fri (03.00 PM - 08.00 PM)
- **FEE:**
- **For Indian Nations:** Rs. 500/- (Faculty / Research Scholar/student/Industry)
- **For Foreigners:** 60US Dollars (Faculty/Research Scholar/ Student/ Industry)

REGISTRATION PROCESS

- Registration fee will be paid through online mode only. The account details for this purpose are as follows:

Account Name: NIT Patna,
Account no: 50380476798
IFSC Code: IDIB000B810
Bank Name: Indian Bank



* Scan the QR code for payment using UPI apps Only

• **Registration form link:**
forms.gle/K4EpKq6cXS9239Dh8

Select institute name as

Malla Reddy College of Engineering And Technology

- A PDF file of the online filled registration form with proof of the paid registration fee has to be emailed to mrcetshwebmail@gmail.com

Last date registration: 30.01.2025

CHIEF PATRON

Sri Ch Malla Reddy, Founder Chairman, MRGI,

PATRONS

Sri Ch Mahender Reddy, Secretary, MRGI,
Dr Ch Bhadra Reddy, President, MRGI,

CONVENORS

Dr V S K Reddy, Director, MRCET
Dr S Srinivasa Rao, Principal, MRCET

CO-CONVENOR

Dr T Venugopal, Dean Student Welfare, MRCET

CO-ORDINATOR

Dr V Madhusudhana Reddy, HOD - H&S

CO-COORDINATORS

Dr V Neeraja, Associate Professor
Dr P Vengal Rao, Associate Professor

ORGANISING COMMITTEE

Dr M Srinivasa Rao, Associate Professor
Dr K Ramakrishna, Associate Professor
Dr A Adithya Prasad, Associate Professor
Dr T Srikanth Reddy, Asst. Professor
Dr P Gangadhar, Asst. Professor
Dr A Eswar Reddy, Asst. Professor
Dr T Navya Kumari, Asst. Professor
Dr K Rajamallu, Asst. Professor
Dr S Nagamani, Asst. Professor

For any queries please contact

Dr. P Vengal Rao, Associate Professor

☎ **77803 87094**

ONE WEEK ONLINE FACULTY DEVELOPMENT PROGRAM

On
**Nanotechnology for
VLSI: Fabrication and Challenges**

Under the banner of

**Electronics and ICT Academy,
National Institute of Technology, Patna**

3rd – 7th February, 2025



Organized by

**DEPARTMENT OF
HUMANITIES AND SCIENCES**

**MALLA REDDY COLLEGE OF
ENGINEERING AND TECHNOLOGY**

(UGC - Autonomous Institution
Approved by AICTE & Affiliated to JNTUH, HYDERABAD)

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Information Technology (MeitY),
Govt. of India

ABOUT MRCET

Malla Reddy College of Engineering and Technology (Autonomous) is approved by AICTE, New Delhi and affiliated to JNT University, Hyderabad. The MRCET College is offering B.Tech Programs in the areas of CSE, CSE-AI&ML, CSE-DS, CSE-CS, CSE-IOT, IT, EEE, ECE, ME, ANE and M.Tech Programs in CSE, ECE, ANE, ME and Master's in Business Administration (MBA). The college also has UGC Autonomous status for both Engineering and Management programs. The College also is accredited by National Board of Accreditation (NBA-Tier-1) and NAAC with 'A' Grade and is also recognized under UGC 2f & 12(B) status. The Institution is certified with ISO 9001:2015. The college has been ranked 'AAAA' Grade among India's Best Engineering College survey by Career360 (outlook Group). The College also ranked among the Top Engineering Colleges of Excellence in Telangana Competition Success Review (CSR). The department of MBA is endowed 9th Best B-School (Other than IIMs) in India.

ABOUT THE DEPARTMENT

The Department of Humanities and Sciences (H&S) has been established in the academic year 2004 with its main objective being "to deliver quality education and instill high patterns of discipline in order to make the students technologically superior and ethically strong thus improving the quality of human life."

The department is founded on the conviction that the Humanities give purpose, direction and value to education and life. Sciences provide a conceptual base in basic sciences which form a foundation to the engineering subjects. As a pillar to all the engineering departments, it comprises of five basic disciplines namely, English & Soft skills, Mathematics, Physics, Chemistry, and Management Sciences.

The Department of Humanities & Sciences plays a pivotal role in inculcating basic scientific knowledge and overall development of the child. It provides an ideal environment for the freshmen students to pursue their engineering by taking advantage of the well-established facilities and expertise available within the department and on-campus.

ABOUT THE PROGRAM

Nanotechnology plays a crucial role in VLSI fabrication by enabling the creation of incredibly small transistors and other electronic components on a single chip, achieved through the manipulation of matter at the atomic and molecular level, allowing for significantly increased circuit density and improved performance in microchips. To achieve these small features, advanced lithography techniques may be employed which use extremely short wavelengths of light to precisely pattern the circuit layout on the wafer. The nanotechnology offers a precise deposition of extremely thin layers of materials which is crucial for the nanoscale structures on the wafer. By the virtue of having smaller transistors, the devices will have faster switching speed which will result in increased computational capability. Moreover, miniaturization reduces power consumption which will increase the durability of the device.

PROGRAM OBJECTIVES

The FDP aims to provide participants with an in-depth understanding of cutting-edge deep learning technique and optimization methods tailored to address challenges in the healthcare domain. The program with focus on equipping faculty and researchers with theoretical knowledge, practical skills, and real-world applications in healthcare technology innovation. Participants will also gain insights into the latest advancements in AI-driven healthcare solutions. The program will foster collaboration and encourage the integration of these technologies to improve healthcare outcomes and efficiency.

- To know the VLSI Fabrication tools
- To know the characterization tools
- To know the fundamentals of nanotechnology
- To know the applications of nanotechnology in VLSI
- To know the application of nanotechnology in optoelectronics devices

TOPICS TO BE COVERED

- Fundamentals of nanotechnology
- Fundamentals of VLSI fabrication.
- Fabrication tools and applications Characterization tools and applications
- Nanomaterial synthesis and applications
- Nanotechnology in semiconductor device
- Optical interconnects
- Fabrication of optoelectronics devices
- Fundamentals of semiconductor quantum nanophotonic
- Challenges and future scope of nanotechnology in device fabrications

RESOURCE PERSONS

- Prof. P. Chakrabarti, IIT BHU
- Prof. Sudeb Dasgupta, IIT Roorkee
- Prof. Jawar Singh, IIT Patna
- Prof. Anchal Srivastava, BHU
- Prof. Govind Gupta, CSIR NPL, New Delhi
- Prof. Mayank Shrivastava, IISc Bangalore
- Prof. Nandita Das Gupta, IIT Madras
- Prof. Shailendra K. Varshney, IIT Kharagpur
- Prof. Shriganesh Prabhu, TIFR, Mumbai
- Dr. Pramod Kumar Tiwari, IIT Patna
- Dr. C. Periasamy, NIT Calicut
- Dr. Amit Verma, IIT Kanpur,
- Dr. Santanu Manna, IIT Delhi
- Dr. Apurba Laha, IIT Bombay and others

PROGRAMME SCHEDULE

Invited Talks					
Session/Date	Monday (3 rd Feb., 2025)	Tuesday (4 th Feb., 2025)	Wednesday (5 th Feb., 2025)	Thursday (6 th Feb., 2025)	Friday (7 th Feb., 2025)
Session I 9 am to 11 am	Prof. Sanjeev Manhas, IIT Roorkee (Advances in nanoscale CMOS technology)	Dr. Shivendra Jaiswal, NIT Patna (Nanomaterial for membrane application)	Prof. Sudeb Dasgupta, IIT Roorkee (Forksheet and Nanosheets for next generation low power computing in beyond Moore Era)	Dr. C. Periasamy, NIT Calicut (Design and developments of FEMT based biosensor)	Prof. P. Chakrabarti, IIT B.H.U. (Fabrication and challenges of semiconductor devices)
11:00 am to 11:15 am	TEA BREAK				
Session II 11:15 am to 01:15 pm	Prof. Mukesh Kumar, IIT Indore (Chip-scale optoelectronic devices based on semiconductor hetero-junctions)	Dr. Shashi Kant Sharma, IIIT Ranchi (Recent trends in semiconductor devices from simulation and integration of machine learning aspects)	Prof. Sanjeev Manhas, IIT Roorkee (LAB-1: Demonstartion of fabrication facilities)	Prof. Anchal Srivastava, BHU (LAB-2: Synthesis and characterization of nanomaterials)	Prof. Jawar Singh, IIT Patna (Device and Circuit for In-memory computing and neuromorphic)
01:15 pm to 01:45 pm	LUNCH				
Session III 01:45 pm to 03:45 pm	Dr. Shashi Kant Sharma, IIIT Ranchi (Emerging research trends in thin film technology based devices for electronics and photonics applications)	Prof. Anchal Srivastava, BHU (Synthesis and characterization of nanomaterials)	Prof. Shailendra K. Varshney, IIT Kharagpur (Fabrication aspects of photonics nanostructure)	Dr. Shivendra Jaiswal, NIT Patna (LAB-3: Nanomaterial for membrane application)	Prof. Mukesh Kumar, IIT Indore (LAB-5: Demonstartion of fabrication and characterizatiof semiconductor photonic devices. lithography and allied facilities)
03:45 pm to 04:00 pm	TEA BREAK				
Session IV 04:00 pm to 06:00 pm	Prof. Govind Gupta, CSIR NPL, New Delhi (Recent Advancements in Emerging and Advanced Optoelectronic Research)	Dr. C. Periasamy, NIT Calicut (Design and development of MEMS based sensor and actuators)	Dr. Sunil Singh Kushvaha, Principal Scientist, CSIR-NPL (Scanning probe microscopy: Seeing and fabrication at nanoscale)	Dr. Pushpa Giri, NIT Patna and Dr. Jitendra Bahadur Maurya, NIT Patna (LAB-4: Demonstartion of sputtering, spin coating, and probe sonicator machines)	Dr. Sunil Singh Kushvaha, Principal Scientist, CSIR-NPL (LAB-6: Demonstartion of pulsed laser deposition and allied systems)
06:00 pm to 06:30 pm	Valedictory Session/Certificate Distribution/Tea				